AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor element having a circuit surface on which a plurality of circuit electrodes are disposed, said circuit surface being coated with a protecting film,

a stress relaxation layer which is formed on the protecting film of the circuit surface of said semiconductor element so as to expose the circuit electrodes, is made of a thermoplastic resin and has an inclination in an edge portion thereof to form an inclined edge portion,

a wiring layer comprised of a plurality of wirings, each of said wirings being connected to one of the circuit electrodes and disposed so as to make an electrical connection from said circuit electrodes, via the edge portion of the stress relaxation layer and to a desired site on a surface of the stress relaxation layer,

a surface protecting film which covers a surface of the wiring layer so as to expose a prescribed portion on each of the plurality of wirings on the surface of the stress relaxation layer, and

an external connection terminal formed by connecting a bump to said prescribed exposed portion of each of the plurality of wirings,

wherein a protuberant portion is formed between the inclined edge portion and a flat portion of the stress relaxation layer and wherein a height of the protuberant portion is slightly higher than a height of the flat portion..

2. (Currently Amended) A semiconductor device according to Claim 1, wherein a protuberant portion is formed in a surrounding part connected to the inclined edge portion of the stress relaxation layer~~, said protuberant portion having a height which is slightly higher than a height of a flat portion of the stress relaxation layer~~, and a deflected portion is formed in the wiring existing on said protuberant portion.

3. (Previously Presented) A semiconductor device according to Claim 1 or 2, wherein a melting temperature Tm of the thermoplastic resin in said stress relaxation layer is not lower than the maximum attainable temperature Tmax in the process of forming said wiring layer and surface protecting layer.

4. (Previously Presented) A semiconductor device according to Claim 1 or 2, wherein a melting temperature Tm of the thermoplastic resin in the stress relaxation layer is not lower than 350°C.

5. (Previously Presented) A semiconductor device according to Claim 1 or 2, wherein glass transition temperature Tg of the thermoplastic resin in said stress relaxation layer is in the range of from 150°C to 400°C.

6. (Previously Presented) A semiconductor device according to Claim 1 or 2, wherein a coefficient of thermal expansion of the thermoplastic resin in said stress relaxation layer is not greater than 200 ppm/°C.

7. (Original) A semiconductor device according to Claim 1 or 2, wherein thickness of said stress relaxation layer is in the range of from about 35 μm to about 150 μm.

8. (Previously Presented) A semiconductor device according to Claim 1 or 2, wherein the thermoplastic resin in said stress relaxation layer is at least one member selected from the group consisting of polyimide, polyamide, polyamide-imide, epoxy, phenolic and silicone.

9. (Original) A semiconductor device according to Claim 1 or 2, wherein the protecting film formed on the semiconductor element is constituted of an inorganic film and an organic film locally formed on said inorganic film.

10. (Previously Presented) A semiconductor device according to Claim 1 or 2, wherein the wirings are formed so that a width of the wiring in the edge portion of said stress relaxation layer is greater than the width of wiring in a flat portion of said stress relaxation layer, at least regarding signal wirings.

11. (Original) A semiconductor device according to Claim 1 or 2, wherein said wiring layer is constituted of an electric power supply film layer contact-bonded to the surface of said stress relaxation layer and a plating film layer.

12. (Currently Amended) A semiconductor device comprising:

a semiconductor element having a plurality of circuit electrodes disposed

thereon and a circuit surface coated with a protecting film,

a stress relaxation layer formed on the protecting film of the circuit surface of said semiconductor element so as to expose the circuit electrodes, which is made of a thermoplastic resin having a glass transition temperature Tg falling in the range of from 150°C to 400°C and has an inclination in an edge portion thereof,

a wiring layer comprised of a plurality of wirings, each of said wirings being connected to one of the circuit electrodes and disposed so as to make an electrical connection from said circuit electrode, via the edge portion of stress relaxation layer and to a desired site on a surface of the stress relaxation layer,

a surface protecting film which covers a surface of the wiring layer so as to expose a prescribed portion on each of the plurality of wirings on the surface of the stress relaxation layer, and

an external connection terminal formed by connecting a bump to said prescribed exposed portion of each of the plurality of exposed wirings,

wherein a protuberant portion is formed between the inclined edge portion and a flat portion of the stress relaxation layer and wherein a height of the protuberant portion is slightly higher than a height of the flat portion..

13. (Previously Presented) A semiconductor device according to Claim 12, wherein a thickness of said stress relaxation layer is in the range of from about 35 μm to about 150 μm.

14. (Original) A mounted structure of semiconductor device constituted by mounting a semiconductor according to any one of Claims 1 to 13 on a circuit

substrate by connecting an external connection terminal of said semiconductor device to an electrode formed on said circuit substrate.

15. – 17. (Canceled)

18. (Currently Amended) A semiconductor device according to claim ~~17~~1, wherein said wirings are formed also on said protuberant portion.

19. (Currently Amended) A semiconductor device according to claim ~~17~~1, wherein said wirings each have a deflected portion on said protuberant portion.

20. (Previously Presented) A semiconductor device according to claim 1, wherein said external connection terminal does not contain lead.

21. (Previously Presented) A semiconductor device according to claim 1, wherein said thermoplastic resin is prepared by coating a varnish on a first electrically insulating film and volatilizing a solvent in the varnish.

22. (Previously Presented) A semiconductor device according to claim 1, wherein in the inclined edge portion of said stress relaxation layer, a wiring shape is different between a signal line and a ground line or between a signal line and an electric source line among said wirings.

23. (Currently Amended) A semiconductor device comprising:

a semiconductor element having an electrode on a surface thereof,

a first electrically insulating film which covers an electrode-formed face of the semiconductor element and has an opening part at a position corresponding to said electrode, and

a second electrically insulating layer formed on said first electrically insulating film,

wherein said second electrically insulating layer relaxes a stress between said semiconductor device and a substrate on which said semiconductor device is to be mounted, and said second electrically insulating layer is comprised of a thermoplastic resin,

wherein a protuberant portion is formed between an inclined portion and a flat portion of the second electrically insulating and wherein a height of the protuberant portion is slightly higher than a height of the flat portion.

24. (Previously Presented) A semiconductor device according to claim 23, wherein an opposite side to the portion connected to said electrode in said wiring has an external connection terminal to be electrically connected to the substrate on which said semiconductor device is to be mounted.

25. (Previously Presented) A semiconductor device according to claim 24, wherein said external connection terminal does not contain lead.

26. (Canceled)

27. (Previously Presented) A semiconductor device according to claim 23, wherein a width of the wiring in an inclined portion of said second electrically insulating is wider than a width of the wiring in a flat portion of said second electrically insulating, regarding a width of the wiring of at least either an electric source or ground of said wirings.

28. (Previously Presented) A semiconductor device according to claim 23, wherein in an inclined portion of said second electrically insulating, the wiring shape is different between a signal line and a ground line or between a signal line and an electric source line.